CLAIMS:

1. A method of incorporating nitrogen into a silicon-oxide-containing layer, comprising:

exposing the silicon-oxide-containing layer to activated nitrogen species from a nitrogen-containing plasma to introduce nitrogen into the layer; the layer being maintained at less than or equal to 400°C during the exposing; and

thermally annealing the nitrogen within the layer to bond at least some of the nitrogen to silicon proximate the nitrogen.

2. The method of claim 1 wherein the layer is maintained at a temperature of from 50°C to 400°C during the exposing.

3. The method of claim 1 wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

4. The method of claim 1 wherein the plasma is maintained with a power of from about 500 watts to about 3000 watts during the exposing.

5. The method of claim 1 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5 mTorr to about 10 mTorr during the exposing.

6. The method of claim 1 wherein the exposing occurs for a time of less than or equal to about 1 minute.

7. The method of claim 1 wherein the exposing occurs for a time of from about 3 seconds to about 1 minute.

8. The method of claim 1 wherein the exposing occurs for a time of from about 10 seconds to about 15 seconds.

9. The method of claim 1 wherein the annealing comprises rapid thermal processing at a ramp rate of at least about 50°C/sec to a temperature of less than 1000°C, with such temperature being maintained for at least about 30 seconds.

10. The method of claim 1 wherein the annealing comprises thermal processing at temperature of less than 1100°C for a time of at least 3 seconds.

11. A method of forming a nitrogen-enriched region within a silicon-oxide-containing layer, comprising:

providing the silicon-oxide-containing layer over a substrate; the layer having an upper surface above the substrate and a lower surface on the substrate;

exposing the layer to activated nitrogen species from a nitrogen-containing plasma to introduce nitrogen into the layer and form a nitrogen-enriched region, the nitrogen enriched region being only in an upper half of the silicon-oxide-containing layer; and

thermally annealing the nitrogen within the nitrogen-enriched region to bond at least some of the nitrogen to silicon proximate the nitrogen; the nitrogen-enriched region remaining confined to the upper half of the silicon-oxide-containing layer during the annealing; the thermal annealing comprising either (1) thermal processing at a temperature of less than 1100°C for a time of at least 3 seconds, or (2) rapid thermal processing at a ramp rate of at least about 50°C/sec to a process temperature of less than 1000°C, with the process temperature being maintained for at least about 30 seconds.

12. The method of claim 11 wherein the nitrogen-enriched region is formed only in the upper third of the silicon-oxide layer by the exposing.

13. The method of claim 11 wherein the nitrogen-enriched region is formed only in the upper third of the silicon-oxide layer by the exposing and remains confined to the upper third of the silicon-oxide containing layer during the annealing.

14. The method of claim 11 wherein the nitrogen-enriched region is formed only in the upper fourth of the silicon-oxide layer by the exposing and remains confined to the upper fourth of the silicon-oxide containing layer during the annealing.

15. The method of claim 11 wherein the nitrogen-enriched region is formed only in the upper fifth of the silicon-oxide layer by the exposing and remains confined to the upper fifth of the silicon-oxide containing layer during the annealing.

16. The method of claim 11 wherein the layer is maintained at a temperature of less than 400°C during the exposing.

17. The method of claim 11 wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

18. The method of claim 11 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5 mTorr to about 10 mTorr during the exposing.

19. The method of claim 11 wherein the exposing occurs for a time of less than or equal to about 1 minute.

20. A method of forming a transistor, comprising:

forming a gate oxide layer over a semiconductive substrate, the gate oxide layer comprising silicon dioxide;

exposing the gate oxide layer to activated nitrogen species from a nitrogen-containing plasma to introduce nitrogen into the layer, the layer being maintained at less than or equal to 400°C during the exposing;

thermally annealing the nitrogen within the layer to bond at least a majority of the nitrogen to silicon proximate the nitrogen;

forming at least one conductive layer over the gate oxide; and

forming source/drain regions within the semiconductive substrate; the source/drain regions being gatedly connected to one another by the conductive layer.

21. The method of claim 20 wherein the conductive layer is formed on the gate oxide.

22. The method of claim 20 wherein the conductive layer is formed after the annealing.

23. The method of claim 20 wherein the source/drain regions are formed after the annealing.

24. The method of claim 20 wherein the conductive layer and source/drain regions are formed after the annealing.

25. The method of claim 20 wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

26. The method of claim 20 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5 mTorr to about 10 mTorr during the exposing.

27. The method of claim 20 wherein the exposing occurs for a time of less than or equal to about 1 minute.

28. The method of claim 20 wherein the annealing comprises thermal processing at temperature of less than 1100°C for a time of at least 3 seconds.

29. A method of forming a transistor, comprising:

forming a gate oxide layer over a semiconductive substrate, the gate oxide layer comprising silicon dioxide; the gate oxide layer having an upper surface and a lower surface;

exposing the gate oxide layer to activated nitrogen species from a nitrogen-containing plasma to introduce nitrogen into the gate oxide layer and form a nitrogen-enriched region, the nitrogen enriched region being only in an upper half of the gate oxide layer;

thermally annealing the nitrogen within the nitrogen-enriched region to bond at least a majority of the nitrogen to silicon proximate the nitrogen; the nitrogen-enriched region remaining confined to the upper half of the silicon-oxide-containing layer during the annealing;

forming at least one conductive layer over the gate oxide layer; and

forming source/drain regions within the semiconductive substrate; the source/drain regions being gatedly connected to one another by the conductive layer.

30. The method of claim 29 wherein the nitrogen-enriched region is formed only in the upper third of the silicon-oxide layer by the exposing.

31. The method of claim 29 wherein the nitrogen-enriched region is formed only in the upper third of the silicon-oxide layer by the exposing and remains confined to the upper third of the silicon-oxide containing layer during the annealing.

32. The method of claim 29 wherein the layer is maintained at a temperature of less than 400°C during the exposing.

33. The method of claim 29 wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

34. The method of claim 29 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5 mTorr to about 10 mTorr during the exposing.

35. The method of claim 29 wherein the exposing occurs for a time of less than or equal to about 1 minute.

36. The method of claim 29 wherein the annealing comprises thermal processing at temperature of less than 1100°C for a time of at least 3 seconds.

37. The method of claim 29 wherein the conductive layer is formed on the gate oxide.

38. The method of claim 29 wherein the conductive layer is formed after the annealing.

39. The method of claim 29 wherein the source/drain regions are formed after the annealing.

40. The method of claim 29 wherein the conductive layer and source/drain regions are formed after the annealing.

41. A transistor structure, comprising:

a gate oxide layer over a semiconductive substrate, the gate oxide layer comprising silicon dioxide; the gate oxide layer having a nitrogen-enriched region which is only in an upper half of the gate oxide layer;

at least one conductive layer over the gate oxide layer; and

source/drain regions within the semiconductive substrate; the source/drain regions being gatedly connected to one another by the conductive layer.

42. The structure of claim 41 wherein the conductive layer comprises conductively-doped silicon.

43. The structure of claim 41 wherein the conductive layer comprises p-type conductively-doped silicon.

44. The structure of claim 41 wherein the nitrogen-enriched region is only in the upper third of the gate oxide layer.

45. The structure of claim 41 wherein the nitrogen-enriched region is only in the upper fourth of the gate oxide layer.

46. The structure of claim 41 wherein the nitrogen-enriched region is only in the upper fifth of the gate oxide layer.

47. The structure of claim 41 wherein the gate oxide layer is at least about 5Å thick, and wherein the nitrogen-enriched region is only in the upper 50% of the gate oxide layer.